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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,691	06/10/2002	Marieanne Almesaker	193778.0026	4816

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EXAMINER	
BONZO, BRYCE P	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/088,691	ALMESAKER ET AL.	
	Examiner	Art Unit	
	Bryce P Bonzo	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 1, 2, 4-9 are rejected under 35 USC §102.

Claims 3, 10, 11 and 14 are rejected 35 USC §103.

Claims 12 and 13 are rejected under 35 USC §112.

Rejections under 35 USC §112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim s 12 and 13 recites the limitation "application" . There is insufficient antecedent basis for this limitation in the claim. These claims refer to what appears to be two different applications stored in two different memories. However the claims begin to use either loosely recite two different application without regard to antecedent basis or refer to the same application stored multiple places in multiple version. The Examiner is unable to determine which is the case. Appropriate clarification to the claims is required to allow examination against the prior art.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Drerup (United States Patent No. 5,333,285).

As per claim 1, Drerup discloses:

processor means (Figure 4, item 21),

an ordinary memory unit connected to said processor mean and arranged to comprise at least one program that is executed by the processor means (Figure 4, item 25);

a supervisory unit that supervises the function of the computer device and that is arranged to, in case an error occurs, send a restart signal or a stop signal to the processor means (Figure 4, item 5),

characterised by

a further memory unit that is arranged to comprise at least some basic system instruction (column 4, lines 19-20), wherein the computer device is arranged such that the processor means always at a restart generated by said restart signal from supervisory unit is connected to the further memory and read and executes instructions that are stored in the same (column 4, lines 19-20 describe initialization code which

must be read prior to continuing any kind of boot), while the ordinary memory unit is disconnected from the processor means (the Examiner interprets the deliberate not reading of the program in RAM as a disconnection), and wherein said further memory unit is arranged to be write protected at least when the computer device is in operation (column 4, lines 19-20: ROM is always write protected).

As per claim 2, Drerup discloses:

wherein the ordinary memory unit and the further memory unit constitute two different, physically separate, memories (Figure 4, items 23 and 25).

As per claim 4, Drerup discloses

wherein said supervisory unit is arranged to generate a signal in dependence of a timer in such a manner that said restart signal is generated if no trigger-signal signal that sets the timer to zero is received with a predetermined time interval (column 4, lines 6-9)

As per claim 5, Drerup discloses:

a memory safety circuit that is arranged to stop the reading from the ordinary memory unit and to connect for reading from said further memory unit when both said restart signal and a signal indicating applied supply voltage is the case (column 4, lines 6-14; the power being supplied signal is inherent as the device will not be functioning without power).

As per claim 6, Drerup discloses:

wherein said further memory unit is arranged such that it comprises basic system instruction with a high degree of reliability (column 4, lines 19-20 and 31-34, POST code is hardened in ROM).

As per claim 7, Drerup discloses:

wherein said further memory unit is arranged such that it comprises system instructions with a degree of reliability that is higher than the degree of reliability that is the case in the ordinary memory unit (ROM 23 is more hardened than the RAM 25).

As per claim 8, Drerup discloses:

wherein at least said further memory unit is a non-volatile memory (ROM is non-volatile by definition).

As per claim 9, Drerup discloses:

wherein said processor means comprises a working memory that is arranged such that a restart of the computer device this memory is reset before reading from said further memory unit is started (column 3, line 44: discloses the use of Intel x86 which have an on-chip cache which qualifies as a working memory, and is reset power any processor reset by design).

Rejections under 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 10, 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drerup (United States Patent No. 5,333,285).

As per claim 3, Drerup does not explicitly disclose:

(wherein the memory units) constitute two parts of physically the same memory, but with different memory addresses. The Examiner takes Official Notice that placing RAM and ROM in the same physical memory element is notoriously well known. This practice well known to reduce the number of chips needed to produce a device, and is often used in embedded devices or devices where large bus structures on the circuit board are disadvantageous. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the well known practice of using ROM and RAM into the system of Drerup in order to reduce the size of the device.

As per claim 10, Drerup does not explicitly disclose:

if restart signal has been generated a predetermined number of times, then in case an error occurs again, said stop signal is generated. Official Notice is taken that is

it notoriously well known by those in the fault tolerant arts to stop restarting a failed system after a certain number of attempts if the device continues to fail. This practice provides multiple benefits. First, it allows a system to skip a faulty device and spend all its effort attempting to restore the device. Second, it prevents a user from using a device which has been determined to irrevocably faulty from being used, and thus prevent future failures. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the well known practice of allowing only a certain number of resets prior to being stopped in to the system of Drerup thereby creating a more robust system capable of handling repetitive severe faults.

As per claim 11, Drerup does not explicitly disclose:

a switching member for manually generating said restart signal. The Examiner takes Official Notice that it is notoriously well known to incorporate manual reset switches. Manually resetting computers is a time proven manner with which to resolve computer problem and is still aggressively practiced in the modern computer environment. This can be simply illustrated by the ubiquitous reset button located on the front of PCs. These buttons allow a user to sense a failure and start the recovery process if the computer fails to detect the failure or if the computer is placed in a state where it is unable to function at all. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the well known manual reset button in to the system of Drerup thus creating a more fault tolerant system as the user can begin a recovery operation.

As per claim 14, Drerup does not explicitly disclose:

a system that is a included in an aircraft. The Examiner takes Official Notice that is it notoriously well known to incorporate fault tolerant architectures in to computer avionics. From simple watchdog timers to robust fail over processors and massive redundancy the fault hardening of avionics is practiced at every level aircraft design. Aircraft pose a serious problem when they fail while in operation. As such extravagant lengths are taken to ensure faults are kept to a minimum. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the fault system of Drerup into an aircraft, thus creating an aircraft which is further hardened against faults and therefore is safer of the passengers, pilots and all involved in the operation of the aircraft.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P Bonzo whose telephone number is (703) 305-4834 or upon moving to the new facilities in Alexandria (571) 272-3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713 or upon moving to the new facilities in Alexandria (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

Bryce P Bonzo
Examiner
Art Unit 2114

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